REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance.

Favorable reconsideration and allowance of the application is respectfully requested.

Applicants assert that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

Status of Claims

Claims 1 – 3, 7 – 12, 16, and 18 - 51 remain pending in the application. Claims 1-51 have been rejected. Claims 4 – 6, 13 – 15 and 17 have been cancelled without prejudice or disclaimer. Applicants reserve all rights to file a divisional or continuation application for the cancelled subject matter. Claims 1, 7, 10, 16 and 18 - 20 have been amended.

Remarks to the Specification

In the office Action, the Examiner stated that the title is not descriptive and requested a new title that is clearly indicative of the invention to which the claims are directed. Accordingly, Applicants have amended the title to be indicative of the invention to which the claims are directed.

Claim Objections

In the Office Action, the Examiner objected to claim 4 because of alleged informalities. Claim 4 has been cancelled and therefore the rejection of this claim is now moot.

CLAIM REJECTIONS

35 U.S.C. § 101 Rejections

Claims 1 - 51 have been rejected under 35 U.S.C. § 101 as allegedly lacking a tangible result.

Applicants have amended the independent method claim, claims 1, 7, 10, 16 and 19 to include at least the operation of executing the micro-operation.

As per the apparatus claims, Applicants respectfully traverse the rejection in view of the following remarks. Each of independent claims 22, 25, 29, 34, 37, 40, 44 and 49 recites, at least, "a processor to execute instructions, the processor comprising: an instruction decoder". Applicants respectfully submit that these elements are tangible elements.

Accordingly, applicant respectfully submits that claims 1, 7, 10, 16, 19, 22, 25, 29, 34, 37, 40, 44 and 49 and their dependent claims are allowable under 35 U.S.C. § 101 and requests that the rejection of claims 1 - 51 under 35 USC 101 be withdrawn.

35 U.S.C. § 102 Rejections

Claims 1 - 21 have been rejected under 35 U.S.C. § 102(b), as being anticipated by Col et al. (US Patent No. 6,330,657). Applicants respectfully traverse the rejection of claims 1 - 21 under 35 U.S.C. § 102(b).

As is well established, in order to successfully assert *a prima facie* case of anticipation, the Examiner must provide a single prior art document that teaches every element and limitation of the claim or claims being rejected.

Independent claim 1 recites "selecting values for a field of said micro-operation based at least upon bits of a field of a micro-operation template stored in a programmable logic array, wherein the number of said bits is fewer than the number of bits in said field of said micro-operation".

Independent claim 7 recites "decoding an instruction into a fused micro-operation" and further "selecting values of a field of said fused micro-operation based solely upon an indication that said instruction is not being decoded into a simple micro operation."

Independent claim 10 recites "receiving an instruction to be decoded into a fused micro-operation" and further "selecting values of a first field of said fused micro-operation based solely both upon an indication that said instruction is not being decoded into a simple micro-operation and upon a value decoded from a field of said micro-operation template that is used to select values of a second field of said fused micro-operation".

Independent claim 16 recites "receiving a first instruction to be decoded into one or more fused micro-operations; addressing a micro-operation template stored in a programmable logic array by said first instruction" and further "receiving a second instruction to be decoded into one or more simple micro-operations; addressing said micro-operation template by said second instruction".

Independent claim 19 recites "receiving an instruction to be decoded into a simple or fused micro-operation" and further "selecting values of a field of said micro-operation from a first set of physical traces if said micro-operation is simple and from a second set of physical traces if said micro-operation is fused".

It is respectfully asserted that Col et al. does not teach or fairly suggest, at least the above recited elements of claims 1, 7, 10, 16 and 19.

Col et al. discloses an apparatus and method for increasing the throughput within a single channel of a pipeline microprocessor by executing pairs of non-conflicting micro instructions in parallel (see col. 3, lines 43 - 46). Col further discloses that many pairs of instructions can be executed in half the time over that required by a conventional microprocessor (see col. 3, lines 58 - 60).

Col is silent, however, in general as to the preceding stage of decoding (translating) the macro instructions into associated micro instructions and in particular, as to "wherein the number of said bits is fewer than the number of bits in said field of said micro-operation", as recited in claim 1.

Col specifically states that the "fetch stage 402, translate stage 404, resister stage 406, and address stage 408, function like that of a conventional microprocessor 100 described with reference to Fig. 1, the difference being that two micro instructions are presented in parallel for execution (see from col. 13, line 55 to col. 14 lines 4 and element 404 of Fig. 4).

Applicants respectfully assert that the "paired micro instructions" of Col cannot be considered to be the "fused micro-operation" of the subject application, as suggested by the Office Action. As described at paragraph [0028] and the exemplary fused micro instruction (2) described at paragraph [0031] of the subject application, an exemplary "fused" u-op may be "a u-op that combines the operations of two simple u-ops and includes two op-codes, one for each operation". The two simple u-ops combined within the fused micro operation cannot be executed in parallel as can the "paired micro instructions" of Col. In fact, the "paired micro instructions" of Col are a pair of non-conflicting simple micro instructions presented together for parallel execution.

Based on the discussion above, applicants submit that Col et al. fails to teach, either expressly or inherently, all the elements of claims 1, 7, 10, 16 and 19. Accordingly, Applicants respectfully assert that independent claims 1, 7, 10, 16 and 19 are allowable over Col et al.

Claims 2, 3, 8, 9, 11, 12, 18, 20 and 21 depend directly or indirectly from one of independent claims 1, 7, 10, 16 and 19 and incorporate all the elements of the claim from which it depends. Therefore, it is respectfully submitted that claims 2, 3, 8, 9, 11, 12, 18, 20 and 21 are patentable, and thus allowable, at least for all the reasons set forth above.

Claims 4 - 6, 13 - 15, and 17 have been cancelled and therefore the rejection of these claims is now moot.

Accordingly, Applicants respectfully request that the rejection of claims 1-21 under 35 U.S.C. § 102(b) be withdrawn.

35 U.S.C. § 103 Rejection Based on Col in view of Moore

Claims 22 - 36 were rejected under 35 U.S.C. 103(a), as being unpatentable over Col in view of Moore (U.S. Patent 4,354,228). Applicants respectfully traverse the rejection of claims 22 - 36 under 35 U.S.C. § 103(a) in view of the remarks that follow.

According to M.P.E.P. §2142, In order to establish a prima facie case of obviousness, the prior art references must teach or suggest all the claim limitations.

According to M.P.E.P. §2142, In order to establish a prima facie case of obviousness, the prior art references must teach or suggest all the claim limitations.

Without conceding the appropriateness of the combination, Applicants respectfully submit that the combination of Col et al. taken with Moore et al. do not meet the requirements of an obviousness rejection, in that the combination at least fails to teach or suggest all the elements of the claimed invention.

Independent claim 22 recites "a programmable logic array to store a micro-operation template to be addressed by an instruction during decoding of said instruction into a fused micro-operation having a particular field" and further "a multiplexer to select values for said particular field based at least upon bits of a field of said micro-operation template, wherein the number of said bits is fewer than the number of bits in said particular field".

Independent claim 25 recites "a programmable logic array to store a micro-operation template to be addressed by an instruction during decoding of said instruction into a fused micro-operation having a particular field" and further "a multiplexer to select values for said particular field based solely upon an indication that said instruction is not being decoded into a simple micro-operation".

Independent claim 29 recites "a programmable logic array to store a micro-operation template to be addressed by an instruction during decoding of said instruction into a fused micro-operation having a particular field" and further "a decoder to decode a value from a field of said micro-operation template" and further "a multiplexer to select values for said particular field based solely upon said value and an indication that said instruction is not being decoded into a simple micro-operation".

Independent claim 34 recites "a programmable logic array to store a micro-operation template to be addressed by one or more instructions that are to be decoded into one or more fused micro-operations and by one or more instructions that are to be decoded into one or more simple micro-operations".

Applicants respectfully submit that neither Col nor Moore, alone or in combination, teach or suggest, at least the above cited elements of claims 22, 25, 29 and 34.

As discussed above Col et al. does not teach or fairly suggest at least decoding (translating) the macro instructions into fused micro-operations as is required in Applicants' independent claims 22, 25, 29 and 34. Moore et al. does not cure the deficiencies of Col et al.

Claims 23, 24, 26 - 28, 30 - 33, 35 and 36 depends directly or indirectly from one of independent claims 22, 25, 29 and 34 and incorporate all the elements of the claim from which it depends. Therefore, it is respectfully submitted that claims 23, 24, 26 - 28, 30 - 33, 35 and 36 are patentable, and thus allowable, at least for all the reasons set forth above.

Accordingly, Applicants respectfully request that the Examiner withdraw the rejection of claims 22-36 under 35 USC §103(a) over Col et al. in view of Moore et al.

35 U.S.C. § 103 Rejection Based on Col in view of Moore and Takeda

Claims 37 - 51 have been rejected under 35 U.S.C. 103(a), as being unpatentable over Col et al. in view of Moore et al. and in further view of Takeda (U.S. Patent 6,643,720).

Specifically, the Examiner contended that it would have been obvious to take the computing system of Col et al. / Moore et al. and utilize a voltage monitor as shown in Takeda.

Applicants respectfully traverse the rejection of claims 37 - 51 under 35 U.S.C. § 103(a) in view of the remarks that follow.

According to M.P.E.P. §2142, In order to establish a prima facie case of obviousness, the prior art references must teach or suggest all the claim limitations.

Without conceding the appropriateness of the combination, Applicants respectfully submit that the combination of Col et al. taken with Moore et al. and Takeda do not meet the requirements of an obviousness rejection, in that the combination at least fails to teach or suggest all the elements of the claimed invention.

Independent claim 37 recites "a programmable logic array to store a micro-operation template to be addressed by an instruction during decoding of said instruction into a fused micro-operation having a particular field" and further "a multiplexer to select values for said particular field based at least upon bits of a field of said micro-operation template, wherein the number of said bits is fewer than the number of bits in said particular field".

Independent claim 40 recites "a programmable logic array to store a micro-operation template to be addressed by an instruction during decoding of said instruction into a fused micro-operation having a particular field" and further "a multiplexer to select values for said particular field based solely upon an indication that said instruction is not being decoded into a simple micro-operation".

Independent claim 44 recites "a programmable logic array to store a micro-operation template to be addressed by an instruction during decoding of said instruction into a fused micro-operation having a particular field" and further "a decoder to decode a value from a field of said micro-operation template" and further "a multiplexer to select values for said particular field based solely upon said value and an indication that said instruction is not being decoded into a simple micro-operation"

Independent claim 49 recites "a programmable logic array to store a micro-operation template to be addressed by one or more instructions that are to be decoded into one or more fused micro-operations and by one or more instructions that are to be decoded into one or more simple micro-operations".

As discussed above with respect to the 35 U.S.C. 103(a) rejection of claims 22 – 36, neither Col et al. nor Moore et al., alone or in combination, teach or fairly suggest similar elements recited by independent claims 37, 40, 44 and 49. Takeda does not cure the deficiencies of the combination of Col and Moore. Therefore, the combination of Col, Moore and Takeda does not render independent claims 37, 40, 44 and 49 obvious.

Claims 38, 39, 41 - 43, 45 - 48, 50, and 51 depends directly or indirectly from one of independent claims 37, 40, 44 and 49 and incorporate all the elements of the claim from which it depends. Therefore, it is respectfully submitted that claims 38, 39, 41 - 43, 45 - 48, 50, and 51 are patentable, and thus allowable, at least for all the reasons set forth above.

Accordingly, Applicants respectfully request that the Examiner withdraw the rejection of claims 37-51 under 35 USC §103(a) over Col et al. in view of Moore et al. and in further view of Takeda be withdrawn.

CONCLUSION

In view of at least the foregoing amendments and remarks, the pending claims are allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

The Office is hereby authorized to charge any fees associated with this paper to deposit account No. 50-3355.

Respectfully submitted,

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